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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/896,882	BHAMIDIPATI ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-14,16-18,24-26 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-14, 16-18, 24-26, and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file:

2. Claims 1-6, 8-14, 16-18, 24-26, and 28-30 are presented for examination. Applicants have canceled claims 7, 15, 19-23 and 27.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 8, 24 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khandekar in view Krakirian, U.S. Patent 6,064,247.

5. As to claim 1, Khandekar teaches a method comprising:

a. receiving a media clock signal (receiving from an AGP device 66 MHz clock at flip-flop 206) [figures 4, 5 and col. 3 lines 58-62];

b. creating a capture pulse to synchronize the media clock signal with a memory clock signal (clock pulse from 100 MHz clock) [figures 4, 5 and col. 8 lines 59-65];

c. storing the media data in a synchronous memory (memory integrated with the time domain of the host bust and the host interface) [col. 1 lines 34-38, col. 2 lines 57-65, and col. 7 lines 49-53];

Specifically, Khandekar teaches transferring data from a clock domain with slower clock to a clock domain with a faster clock. Khandekar teaches that main memory is synchronous with

the processors speed of the faster clock domain. Khandekar teaches that data would be transferred from the slow clock domain, such as AGP Graphics having 66 MHz clock, to the fast clock domain, such as the main memory.

Khandekar further teaches wherein said creating a capture pulse to synchronize the media clock signal comprises creating a capture. Specifically, Khandekar only discusses using a 100 MHz clock generator to generate clock signals that are used as the capture pulse to [figures 4, 5 and col. 8 lines 58-65]. The clock generator of Khandekar is produced from a common oscillator that also produces a 66 MHz clock. Khandekar does not discuss the details of how the capture pulse is produced. Khandekar does not disclose creating a capture pulse with asynchronous logic.

Krakirian teaches creating a creating a clock with asynchronous logic [figures 6A and 8]. Specifically, Krakirian teaches using asynchronous logic to generate a plurality of clock signal. Krakirian teaches a clocking method that produces a plurality of clocks that would applicable in Khandekar. Further, the clocking method of Krakirian allows synchronization of operations by different logic elements operating at different frequencies [col. 1 lines 54-61].

It would have been obvious to one of ordinary skill in the art, having the teachings of Khandekar and Krakirian before him at the time the invention was made, to modify the common oscillator of Khandekar with the multiple frequency clock generator of Krakirian. One of ordinary skill would have make the modification to achieve synchronization of operations of different logic elements operating at different frequencies in view of the teaching of Krakirian.

6. As to claim 8, Khandekar together with Krakirian taught the method according to claim 1 as described above. Khandekar further teaches wherein said creating a capture pulse to

synchronize the media clock signal comprising creating a capture pulse to synchronize the media clock signal with a transition of the memory clock signal.

7. As to claims 24 and 28, Khandekar together with Krakirian taught the claimed method therefore he also taught the claimed medium containing executable instructions.

8. Claims 2-6, 9, 25-26 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khandekar and Krakirian in view Melo et al., U.S. Patent 6,279,087.

9. As to claim 2, Khandekar together with Krakirian taught the method according to claim 1 as described above. Khandekar together with Krakirian fails to discuss further comprising scheduling to store the media data in synchronous memory. Khandekar only teaches storing media data in synchronous memory.

Melo teaches scheduling to store media data (from different devices such as an AGP, PCI, CPU and other interfaces) in synchronous memory (using an arbiter to multiplexed data paths using priority) [figure 6A and col. 17 line 52 through col. 18 line 6]. Melo teaches a system similar to that of Khandekar. Both systems send media data from devices such as AGP, PCI, and CPUs. Melo further teaches scheduling the storing of media data to allow fair access for all interfaces with priority [col. 17 lines 52-57]. Furthermore, the system of Melo achieves the advantage of maintaining system coherency and improved performance [col. 2 line 60-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of Khandekar and Melo before him at the time the invention was made to modify the controller of Khandekar to include the scheduling of storing media data in the synchronous memory as taught by Melo in order to schedule the storing of media data.

One of ordinary skill in the art would be motivated to make this modification to achieve the advantages of system coherency, improved performance and allow fair access to all interfaces in view of Melo. The advantages would be highly desirable in Khandekar.

10. As to claim 3, Khandekar together with Krakirian and Melo taught the method according to claim 2 as described above. Khandekar teaches storing the media data based on a capture pulse. Melo teaches scheduling to store the media data. It would have been obvious to one of ordinary skill in the art at the time of the invention to schedule to store the media data comprises initiating a signal based upon a capture pulse. In other words, it would have been obvious to one of ordinary skill, having Khandekar and Melo before him, to initiate a signal (to store the media signal) based upon the capture pulse (as taught by Khandekar) when the media data is scheduled to be stored (as taught by Melo).

11. As to claim 4, Khandekar together with Krakirian taught the method according to claim 1 as described above. Kandekar together with Krakirian fails to discuss the method further comprising multiplexing to store the media data in the synchronous memory. Khandekar only teaches storing media data in synchronous memory.

Melo teaches multiplexing to store the media data in synchronous memory [figure 6A and col. 18 lines 3-6]. Specifically, Melo teaches using multiplexed data paths to store media data in synchronous memory. Melo teaches a system similar to that of Khandekar. Both systems send media data from devices such as AGP, PCI, and CPUs. Melo further teaches multiplexing the storing of media data to allow fair access for all interfaces with priority [col. 17 lines 52-57]. In summary, the system of Melo teaches lower level details of data transfer. Furthermore, the

system of Melo achieves the advantage of maintaining system coherency and improved performance [col. 2 line 60-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of Khandekar and Melo before him at the time the invention was made to modify the controller of Khandekar to include the multiplexing to store media data in the synchronous memory as taught by Melo in order to select the paths for storing of media data.

One of ordinary skill in the art would be motivated to make this modification to achieve the advantages of system coherency, improved performance and allow fair access to all interfaces in view of Melo. The advantages would be highly desirable in Khandekar.

12. As to claim 5, Kandekar together with Krakirian and Melo taught the method according to claim 4 as described above. Melo further teaches wherein multiplexing to store the media data comprises receiving a write select signal (arbiter selects which media will write to memory) to store the media data [figure 6A, col. 16 lines 15-18 and col. 18 lines 3-6].

13. As to claims 6 and 9, Khandekar together with Krakirian taught the method according to claim 1 as described above. Khandekar discloses receiving a media clock signal (as set forth above). Khandekar together with Krakirian fails to disclose that the media clock signal comprises receiving a clock signal of a queue comprising data to capture. Specifically, Khandekar only teaches that data will be received on the transition of a capture pulse.

Melo teaches receiving a queue comprising data to capture (receiving data in write data queue 602) [col. 15 lines 35-36]. In using the data queues, Melo teaches that data is sent in queues.

Melo teaches a system similar to that of Khandekar. Both systems send media data from devices such as AGP, PCI, and CPUs. Melo further teaches multiplexing the storing of media data to allow fair access for all interfaces with priority [col. 17 lines 52-57]. In summary, the system of Melo teaches lower level details of data transfer. Furthermore, the system of Melo achieves the advantage of maintaining system coherency and improved performance [col. 2 line 60-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of Khandekar and Melo before him at the time the invention was made to modify the controller of Khandekar to include the multiplexing to store media data in the synchronous memory as taught by Melo in order to select the paths for storing of media data. The data in the queues would be received on the transition of the 100 MHz clock signal used to as a capture pulse.

One of ordinary skill in the art would be motivated to make this modification to achieve the advantages of system coherency, improved performance and allow fair access to all interfaces in view of Melo. The advantages would be highly desirable in Khandekar.

14. As to claims 25-26 and 28-29, Khandekar together with Krakirian and Melo taught the claimed method therefore he also taught the claimed medium containing executable instructions.

15. Claims 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khandekar in view Melo et al., U.S. Patent 6,279,087.

16. As to claim 11, Khandekar taught an apparatus comprising:

a. a synchronizer (transfer logic 38) [figures 1, 5 and col. 3 lines 26-29];

b. synchronous memory (main memory 22) [figure 1 and col. 2 lines 57-65];

Khandekar further taught wherein synchronizer (transfer logic 38) comprises an asynchronous state machine [figures 1, 3, 6 and col. 3 lines 20-33]. The synchronizer of Khandekar comprises among other things delay logic, multiplexing logic, clock generation logic and masking logic all of which contain asynchronous logic. The delay logic and multiplexing logic are asynchronous state machines.

Khandekar does not expressly disclose a buffer coupled to said synchronizer and synchronous memory. Khandekar discloses that the synchronizer is coupled to the synchronous memory through a memory interface. Khandekar does not discuss the details of the memory interface.

Melo teaches a buffer (buffer 416) coupled to synchronous memory (to main memory 104) [figures 3, 4A, 5, 6A and 8A]. As set forth hereinabove, Melo teaches a system similar to that of Khandekar with advantages.

It would have been obvious to one of ordinary skill in the art, having the teachings of Khandekar and Melo before him to modify the memory interface disclosed by Khandekar to include a buffer as taught by Melo in order to temporarily hold data.

One of ordinary skill in the art would be motivated to make this modification to achieve the advantages of system coherency, improved performance and allow fair access to all interfaces in view of Melo. The advantages would be highly desirable in Khandekar.

17. As to claim 12, Khandekar together with Melo taught the apparatus according to claim 11 as discussed above. Melo further taught a multiplexer (multiplexed data paths 615) coupled to more than one buffer [figure 6A and col. 18 lines 3-6]. The data paths are coupled to CPU, PCI,

AGP interfaces which each contain buffers (308, 414, 416, 418, 506,and 508) [figures 3, 4A and 5].

18. As to claim 13, Khandekar together with and Melo taught the apparatus according to claim 11 as discussed above. Melo further taught a scheduler (Memory Queue Arbiter 626 and Queue Memory Control Unit 624) coupled to said synchronous memory [col. 17 line 52 through col. 18 line9, figures 6A and 8A].

19. As to claim 14, Khandekar together with Melo taught the apparatus according to claim 11 as discussed above. Melo further taught an inbound register (Write Data Queue 602) coupled to said buffer [figure 6A].

20. As to claim 15, Khandekar together with Melo taught the apparatus according to claim 11 as discussed above.

21. As to claim 16, Khandekar together with Melo taught the apparatus according to claim 11 as described above. Melo further taught wherein said buffer comprises a buffer to capture data from and inbound register (read request queue) [col. 5 lines 34-45 and figures 3, 4A, 5, 6A]. Melo teaches that data may be sent to and from memory. Therefore, the buffer captures data from an inbound register.

22. As to claim 17, Khandekar together with Melo taught the apparatus according to claim 11 as discussed above. Melo further teaches that the synchronous memory comprises a synchronous random access memory [col. 4 lines 62-64].

23. As to claim 18, Khandekar together with Melo taught the apparatus according to claim 11 as discussed above. Melo further taught wherein said synchronous memory (memory 104)

comprises memory to store data from an inbound register (Write Data Queue) [figures 6A and 8A].

24. Claims 10 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khandekar and Krakirian in view Heuring and Jordan, "Computer System Design and Architecture" (Hereinafter Heuring).

25. As to claim 10, Khandekar together with Krakirian taught the method according to claim 1 as described above. Khandekar does not expressly disclose wherein storing the data in a synchronous memory comprises writing a memory word to the synchronous memory. Khandekar teaches only that a signal that comprises data would be transferred to synchronous memory. Khandekar fails to discuss how the data is arranged.

Heuring teaches that data may be sent to a memory in many forms. Data may be sent as bits, bytes, half-words, words etc. [page 307 first paragraph of section 7.1.1]. The teachings of Heuring are directed toward a generic memory and can be reasonably applied to any type of memory. Heuring suggests to one of ordinary skill in the art that data may be send as a word because when using a word the transmitted data does not have to be reassembled or disassembled by the CPU which would increase processing speed.

It would have been obvious to those of ordinary skill in the art would having the teachings of Khandekar and Heuring before them at the time of the invention to implement the writing of memory word to synchronous memory as taught by Heuring in the memory of Khandekar. One of ordinary skill would have done so that the transmitted data does not have to be reassembled or disassembled by the CPU to increase processing speed.

26. As to claim 30, Khandekar together with Krakirian and Heuring taught the claimed method therefore together they also taught the claimed medium containing executable instructions.

Response to Arguments

27. Applicant's arguments with respect to claims 1-6, 8-14, 16-18, 24-26, and 28-30 have been fully considered but they are not persuasive.

28. Applicants argue in substance with respect to claims 1 and 24, that Krakirian does not teach a "method... **comprising** creating a capture pulse with asynchronous logic to synchronize ...". Applicants further point the abstract of Krakirian on lines 6-8, and at col. 1, lines 54-57 for showing that Krakirian does not have asynchronous logic to create a capture pulse to synchronize clock signals.

In response to applicant's argument with respect to the abstract at lines 6-8, the examiner does not agree with the applicants. This portion of Karkiran only describes that rising edges of all clock signals are synchronized and each clock signal has an approximate duty cycle of 50%. There is nothing in the abstract that describes the type of logic used in Krakirian.

In response to the applicant's argument with respect to the lines recited at col. 1, lines 54-57, the examiner does not agree with the applicants. These lines describe how prior art solved the problem of synchronization. Krakirian is an improvement upon the prior and again these portions of the reference do not describe the type logic used in Krakirian.

The examiner does not disagree that Krakirian uses synchronous logic in creating a capture pulse to synchronize signals. However, Krakirian also uses asynchronous logic as well.

As addressed in the last office action reference was made to figures 6A and 8 of Krakirian, as acknowledged by applicants. Figure 6A shows logic gates 670 (XNOR gate) and 680 (NOR gate) in order to create a capture pulse (other clock signals). Similarly, figure 8 shows logic gates 810, 820 and 830 (inverter). All of these gates are asynchronous logic gates. That is, the inputs for these logic devices do not take input directly from a clock in order to enable an output. As used in Krakirian, they simply output a signal in response to the inputs.

In summary, Krakirian uses both synchronous logic gates and asynchronous logic gates in order to create a capture pulse to synchronize signals. The claims recite "[a] method, comprising:" and thus do not limit what types of other logic may be incorporated in the method or machine-readable medium.

29. Applicants argue in substance with respect to claims 11, that Kandekar does not describe using an asynchronous state machine. The examiner does not agree. As previously addressed, reference was made to figures 1, 3 and 5. Figure 3 show a synchronizer that contains delay elements 122, 108 and 130. These delay elements are asynchronous logic. Further, figure 3 shows a multiplexer 112, which an asynchronous state machine, as its output is not dependent upon a single clock to enable an output at the same time as another output. Figure 5 shows an asynchronous state machine (mask logic) used to enable an output based on skew between two different clocks. Because it is based on skew between two different clocks, the mask logic must be asynchronous. Therefore, Kandekar discloses a synchronizer with an asynchronous state machine.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

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James Trujillo
January 21, 2005

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